## REMARKS

Favorable consideration of the above-identified patent application in light of the foregoing amendment and the following remarks is respectfully requested.

Applicant voluntarily amends independent Claims 1 and 7 to incorporate the limitations of respective dependent Claims 3 and 9 (now canceled); the dependency of Claims 4 and 10 is changed accordingly; minor formal wording changes are also made to various claims, also for reasons not related to patentability; and "device" Claims 16-26 are newly presented for consideration in a first Office Action.

An early and favorable Office Action on the merits is requested.

Respectfully submitted,

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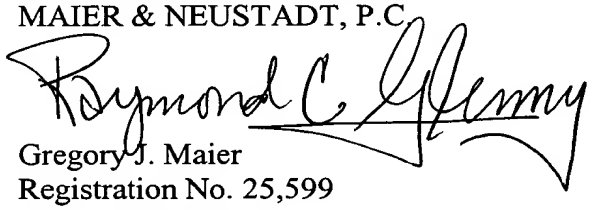

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ATTACHMENT

SHOWING CHANGES TO APPLICATION

1. (Amended) An electrode contact section incorporated in a semiconductor device, comprising:

~~a first-conductivity-type semiconductor substrate;~~

a second-conductivity-type impurity layer formed in one surface of the semiconductor substrate and having a thickness of not more than 1.0 μm from a surface of the semiconductor substrate;

a second-conductivity-type contact layer formed in the impurity layer and having a thickness of not more than 0.2 μm from the surface of the semiconductor substrate, the contact layer being thinner than the impurity layer and having a higher impurity concentration than the impurity layer; [and]

a first electrode formed on the contact layer; and

a second electrode formed at another surface side of the semiconductor substrate for allowing a current to flow between the first and second electrodes.

2. (Amended) The electrode contact section according to claim 1, wherein:

the impurity layer is provided for carrier injection from the impurity layer to the semiconductor substrate, and

the contact layer is provided for reducing a contact resistance between the first electrode and the impurity layer and not for carrier injection.

*3. (canceled)*

4. (Amended) The electrode contact section according to claim [3] 1, wherein the semiconductor device is an insulated gate bipolar transistor (IGBT).

6. (Amended) The electrode contact section according to claim 1, wherein the impurity layer is formed in a portion [of] smaller than the entire one surface of the semiconductor substrate.

7. (Amended) An electrode contact section incorporated in a semiconductor device, comprising:

a first-conductivity-type semiconductor substrate;

a second-conductivity-type impurity layer formed in one surface of the semiconductor substrate;

a second-conductivity-type contact layer formed in the impurity layer, the contact layer being thinner than the impurity layer and having a higher impurity concentration than the impurity layer;

a first electrode formed on the contact layer; [and]

a silicide layer formed between the first electrode and the contact layer, the silicide layer having a contact-layer-side end thereof made to substantially correspond to that portion of the contact layer[,] at which a concentration profile of the contact layer assumes a peak value; and

a second electrode formed at another surface side of the semiconductor substrate for allowing a current to flow between the first and second electrodes.

8. (Amended) The electrode contact section according to claim 7, wherein:

the impurity layer is provided for carrier injection from the impurity layer to the semiconductor substrate, and

the contact layer is provided for reducing a contact resistance between the first electrode and the impurity layer and not for carrier injection.

*9. (canceled)*

10. (Amended) The electrode contact section according to claim [9] 7, wherein the semiconductor device is an insulated gate bipolar transistor (IGBT).

13. (Amended) The electrode contact section according to claim 7, wherein:

the silicide layer has a thickness of not more than 0.2 μm from a surface of the semiconductor substrate, and

the silicide layer is thinner than the contact layer.

15. (Amended) The electrode contact section according to claim 7, wherein the impurity layer is formed in a portion [of] smaller than the entire one surface of the semiconductor substrate.

*Add the following new claims:*

16. (New) A semiconductor device comprising:

a first-conductivity-type semiconductor substrate;

a second-conductivity-type base region formed in a surface of the semiconductor substrate;

a first-conductivity-type impurity region formed in the base region;

a first electrode connected to the first-conductivity-type impurity region;

a gate electrode connected to the base region via an insulation film;

a second-conductivity-type impurity region formed in the surface of the semiconductor substrate and having a thickness of not more than 1.0 μm from the surface of the semiconductor substrate;

a second-conductivity-type contact region formed in the second-conductivity-type impurity region and having a thickness of not more than 0.2 μm from the surface of the semiconductor substrate, the contact region being thinner than the second-conductivity-type impurity region and having a higher impurity concentration than the second-conductivity type impurity region; and

a second electrode formed on the contact region.

17. (New) The semiconductor device according to claim 16, wherein:

the second-conductivity-type impurity region is provided for carrier injection from the second-conductivity-type impurity region to the semiconductor substrate, and

the contact region is provided for reducing a contact resistance between the second electrode and the second-conductivity-type impurity region and not for carrier injection.

18. (New) The semiconductor device according to claim 16, wherein the second-conductivity-type impurity region is formed in the entire surface of the semiconductor substrate.

19. (New) The semiconductor device according to claim 16, wherein the impurity region is formed in a portion less than the entire surface of the semiconductor substrate.

20. (New) A semiconductor device comprising:

a first-conductivity-type semiconductor substrate;

a second-conductivity-type base region formed in a surface of the semiconductor substrate;

a first-conductivity-type impurity region formed in the base region;

a first electrode connected to the first-conductivity-type impurity region;

a gate electrode connected to the base region via an insulation film;

a second-conductivity-type impurity region formed in the surface of the semiconductor substrate;

a second-conductivity-type contact region formed in the impurity region, the second-conductivity-type contact region being thinner than the second-conductivity-type impurity region and having a higher impurity concentration than the second-conductivity-type impurity region;

a second electrode formed on the contact region; and

a silicide region formed between the second electrode and the contact region, the silicide region having a contact-region-side end thereof made to substantially correspond to that portion of the contact region at which a concentration profile of the contact region assumes a peak value.

21. (New) The semiconductor device according to claim 20, wherein:

the second-conductivity-type impurity region is provided for carrier injection from the second-conductivity-type impurity region to the semiconductor substrate, and

the contact region is provided for reducing a contact resistance between the second electrode and the second-conductivity-type impurity region and not for carrier injection.

22. (New) The semiconductor device according to claim 20, wherein the second-conductivity-type impurity region has a thickness of not more than 1.0 μm from the surface of the semiconductor substrate.

23. (New) The semiconductor device according to claim 20, wherein the contact region has a thickness of not more than 0.2 μm from the surface of the semiconductor substrate.

24. (New) The semiconductor device according to claim 20, wherein:

the silicide region has a thickness of not more than 0.2 μm from the surface of the semiconductor substrate, and

the silicide layer is thinner than the contact region.

25. (New) The semiconductor device according to claim 20, wherein the second-conductivity-type impurity region is formed in the entire surface of the semiconductor substrate.

26. (New) The semiconductor device according to claim 20, wherein the second-conductivity-type impurity region is formed in a portion less than the entire surface of the semiconductor substrate.